ANALOG DEVICES

Ultralow Noise, High Speed, BiFET Op Amp

AD745

FEATURES

ULTRALOW NOISE PERFORMANCE
2.9 nV/$\sqrt{Hz}$ at 10 kHz
0.38 μV p-p, 0.1 Hz to 10 Hz
6.9 fA/$\sqrt{Hz}$ Current Noise at 1 kHz

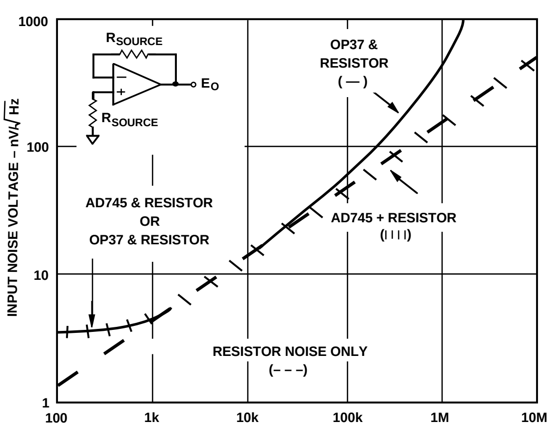
EXCELLENT AC PERFORMANCE
12.5 V/μs Slew Rate
20 MHz Gain Bandwidth Product
THD = 0.0002% @ 1 kHz
Internally Compensated for Gains of +5 (or –4) or Greater

EXCELLENT DC PERFORMANCE
0.5 mV max Offset Voltage
250 pA max Input Bias Current
2000 V/mV min Open Loop Gain
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS
Sonar
Photodiode and IR Detector Amplifiers
Accelerometers
Low Noise Preamplifiers
High Performance Audio

PRODUCT DESCRIPTION

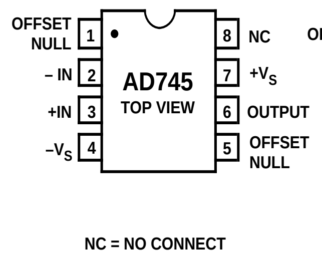
The AD745 is an ultralow noise, high speed, FET input operational amplifier. It offers both the ultralow voltage noise and high speed generally associated with bipolar input op amps and the very low input currents of FET input devices. Its 20 MHz bandwidth and 12.5 V/μs slew rate makes the AD745 an ideal amplifier for high speed applications demanding low noise and high dc precision. Furthermore, the AD745 does not exhibit an output phase reversal.



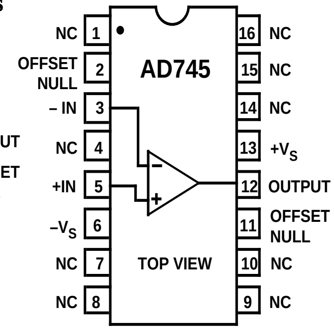
REV. C

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) & 8-Pin Cerdip (Q) Packages



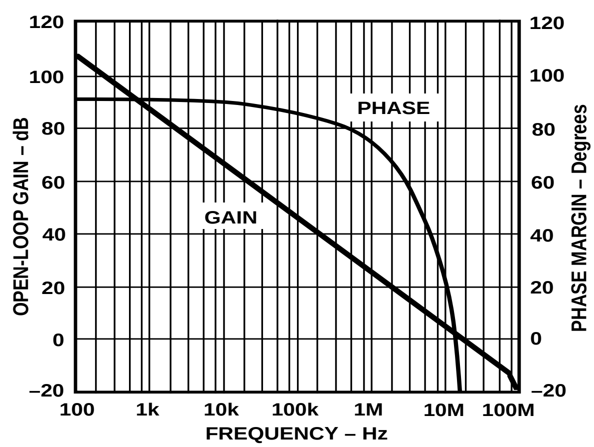
16-Pin SOIC (R) Package



The AD745's guaranteed, tested maximum input voltage noise of 4 nV/$\sqrt{Hz}$ at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is its maximum 1.0 μV p-p noise in a 0.1 Hz to 10 Hz bandwidth. The AD745 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier where low level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains. The AD745 is available in five performance grades. The AD745J and AD745K are rated over the commercial temperature range of 0°C to +70°C. The AD745A and AD745B are rated over the industrial temperature range of –40°C to +85°C. The AD745S is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD745 is available in 8-pin plastic mini-DIP, 8-pin cerdip, 16-pin SOIC, or in chip form.



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Tel: 617/329-4700 Fax: 617/326-8703

AD745–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	Min	AD745J/A Typ	Max	Units
INPUT OFFSET VOLTAGE[1]					
Initial Offset			0.25	1.0/0.8	mV
Initial Offset	T_{MIN} to T_{MAX}			1.5	mV
vs. Temp.	T_{MIN} to T_{MAX}		2		µV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		dB
vs. Supply (PSRR)	T_{MIN} to T_{MAX}	88			dB
INPUT BIAS CURRENT[3]					
Either Input	V_{CM} = 0 V		150	400	pA
Either Input @ T_{MAX}	V_{CM} = 0 V			8.8/25.6	nA
Either Input	V_{CM} = +10 V		250	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	150	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V			2.2/6.4	nA
FREQUENCY RESPONSE					
Gain BW, Small Signal	G = –4		20		MHz
Full Power Response	V_O = 20 V p-p		120		kHz
Slew Rate	G = –4		12.5		V/µs
Settling Time to 0.01%			5		µs
Total Harmonic Distortion[4]	f = 1 kHz, G = –4		0.0002		%
INPUT IMPEDANCE					
Differential			$1 \times 10^{10} \parallel 20$		Ω‖pF
Common Mode			$3 \times 10^{11} \parallel 18$		Ω‖pF
INPUT VOLTAGE RANGE					
Differential[5]			±20		V
Common-Mode Voltage			+13.3, –10.7		V
Over Max Operating Range[6]		–10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		dB
	T_{MIN} to T_{MAX}	78			dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.38		µV p-p
	f = 10 Hz		5.5		nV/√Hz
	f = 100 Hz		3.6		nV/√Hz
	f = 1 kHz		3.2	5.0	nV/√Hz
	f = 10 kHz		2.9	4.0	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		6.9		fA/√Hz
OPEN LOOP GAIN	V_O = ±10 V				
	R_{LOAD} ≥ 2 kΩ	1000	4000		V/mV
	T_{MIN} to T_{MAX}	800			V/mV
	R_{LOAD} = 600 Ω		1200		V/mV
OUTPUT CHARACTERISTICS					
Voltage	R_{LOAD} ≥ 600 Ω	+13, –12			V
	R_{LOAD} ≥ 600 Ω		+13.6, –12.6	V	
	T_{MIN} to T_{MAX}	+12, –10			V
	R_{LOAD} ≥ 2 kΩ	±12	+13.8, –13.1	V	
Current	Short Circuit	20	40		mA
POWER SUPPLY					
Rated Performance			±15		V
Operating Range		±4.8		±18	V
Quiescent Current			8	10.0	mA
TRANSISTOR COUNT	# of Transistors		50		

NOTES

[1] Input offset voltage specifications are guaranteed after 5 minutes of operations at T_A = +25°C.

[2] Test conditions: $+V_S$ = 15 V, $-V_S$ = 12 V to 18 V and $+V_S$ = 12 V to +18 V, $-V_S$ = 15 V.

[3] Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[4] Gain = –4, R_L = 2 kΩ, C_L = 10 pF.

[5] Defined as voltagc between inputs, such that neither exceeds ±10 V from common.

[6] The AD745 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package . . . . 1.3 W
  Cerdip Package . . . . 1.1 W
  SOIC Package . . . . 1.2 W
Input Voltage . . . . $\pm V_S$
Output Short-Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Operating Temperature Range
  AD745J/K . . . . 0°C to +70°C
  AD745A/B . . . . –40°C to +85°C
  AD745S . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 100°C/W, θ_{JC} = 50°C/W
8-Pin Cerdip Package: θ_{JA} = 110°C/W, θ_{JC} = 30°C/W
8-Pin Plastic SOIC Package: θ_{JA} = 100°C/W, θ_{JC} = 30°C/W

ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL-STD-883C has been performed on the AD745, which is a class 1 device. Using an IMCS 5000 automated ESD tester, the two null pins will pass at voltages up to 1000 volts, while all other pins will pass at voltages exceeding 2500 volts.

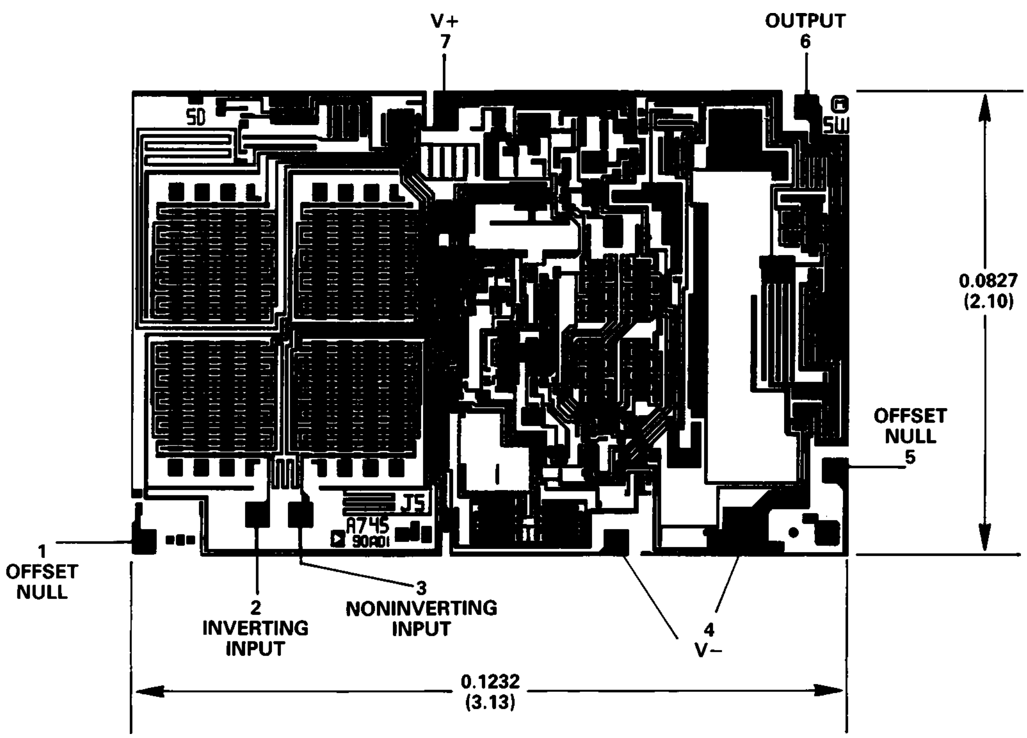
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD745JN	0°C to +70°C	N-8
AD745AN	–40°C to +85°C	N-8
AD745JR-16	0°C to +70°C	R-16

*N = Plastic DIP; R = Small Outline IC.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



AD745 –Typical Characteristics (@ + 25°C, V_S = ±15 V unless otherwise noted)

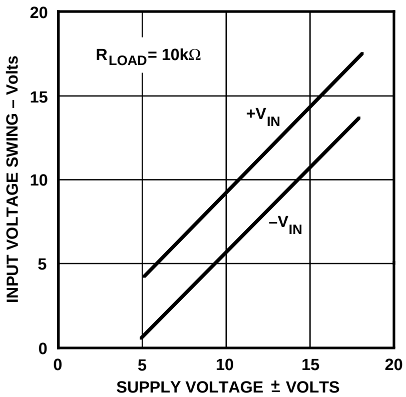


Figure 1. Input Voltage Swing vs. Supply Voltage

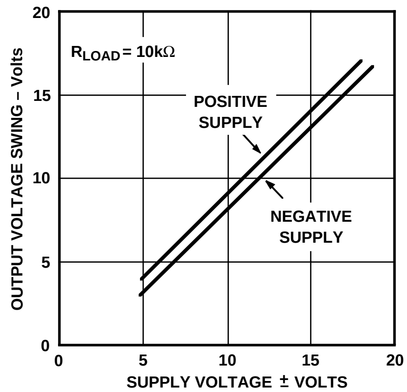


Figure 2. Output Voltage Swing vs. Supply Voltage

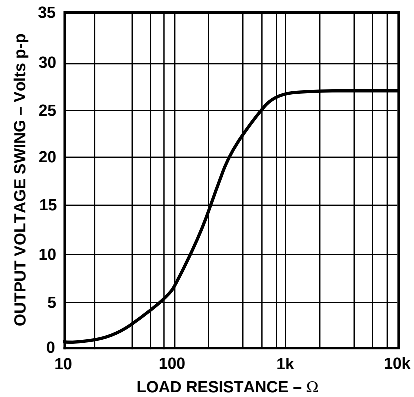


Figure 3. Output Voltage Swing vs. Load Resistance

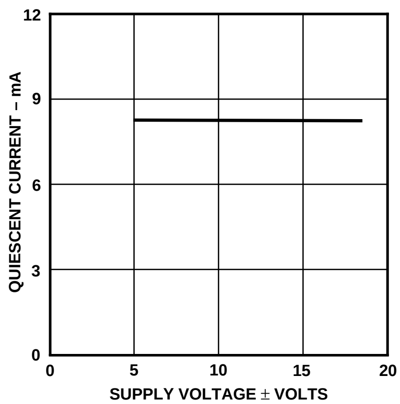


Figure 4. Quiescent Current vs. Supply Voltage

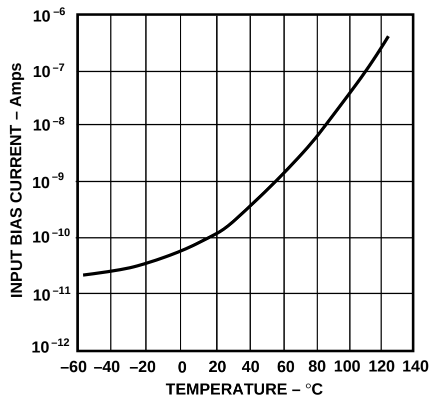


Figure 5. Input Bias Current vs. Temperature

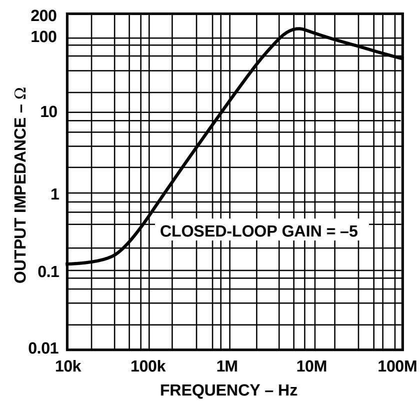


Figure 6. Output Impedance vs. Frequency

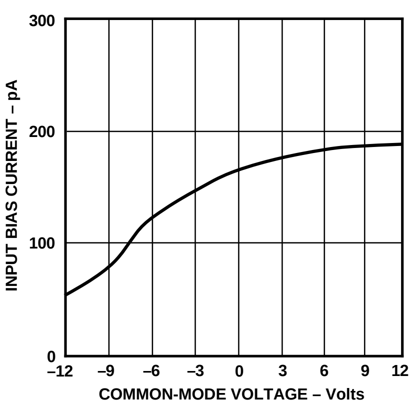


Figure 7. Input Bias Current vs. Common-Mode Voltage

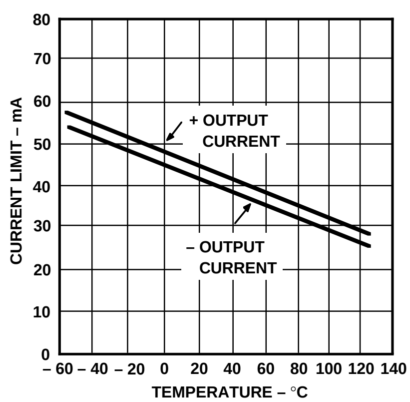


Figure 8. Short Circuit Current Limit vs. Temperature

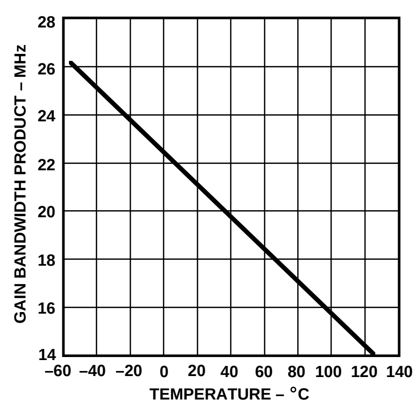


Figure 9. Gain Bandwidth Product vs. Temperature

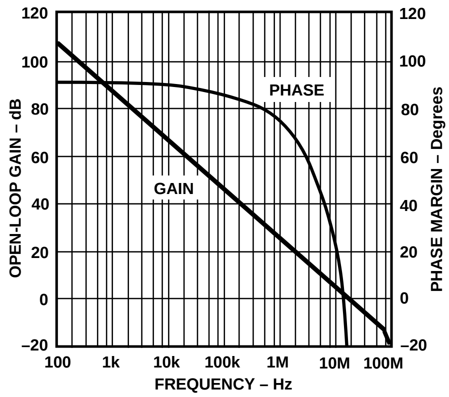


Figure 10. Open-Loop Gain and Phase vs. Frequency

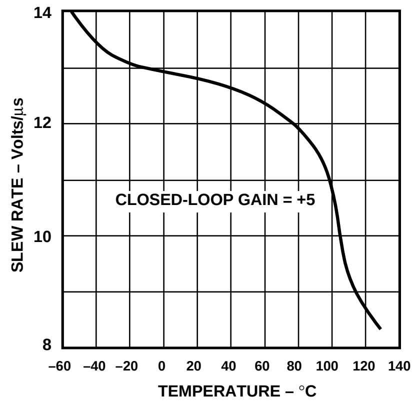


Figure 11. Slew Rate vs. Temperature

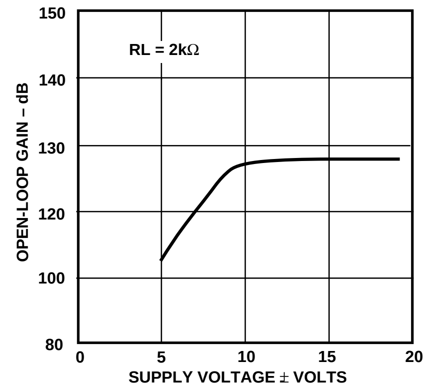


Figure 12. Open-Loop Gain vs. Supply Voltage

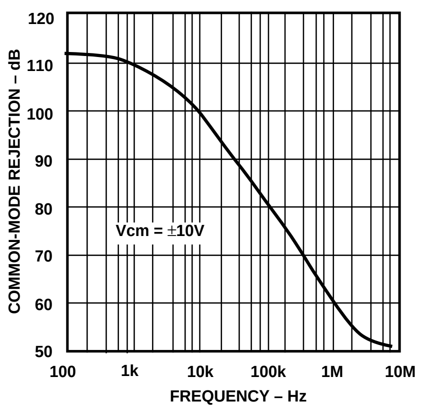


Figure 13. Common-Mode Rejection vs. Frequency

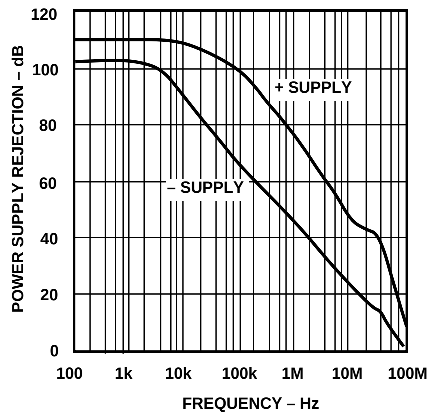


Figure 14. Power Supply Rejection vs. Frequency

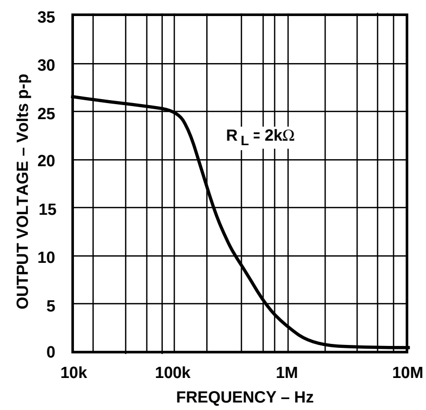


Figure 15. Large Signal Frequency Response

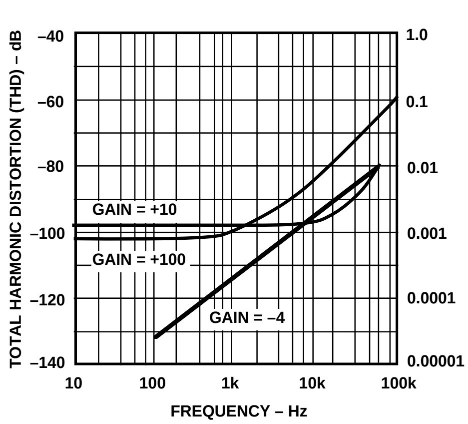


Figure 16. Total Harmonic Distortion vs. Frequency

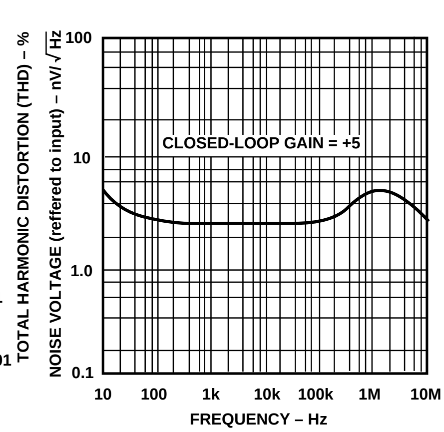


Figure 17. Input Noise Voltage Spectral Density

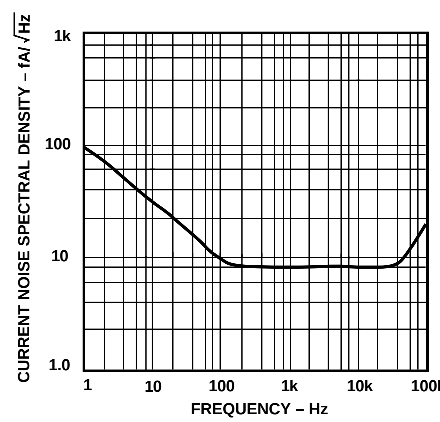


Figure 18. Input Noise Current Spectral Density

AD745–Typical Characteristics

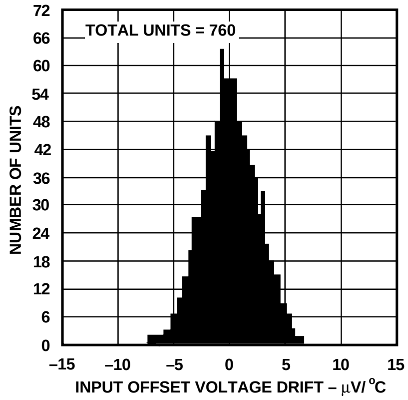


Figure 19. Distribution of Offset Voltage Drift. T_A = +25°C to +125°C

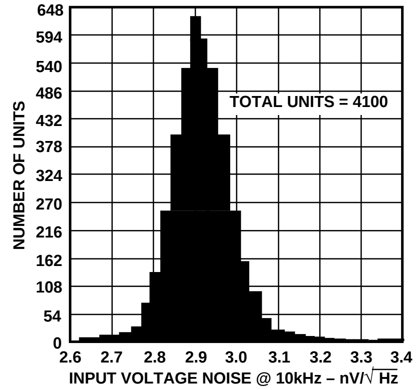


Figure 20. Typical Input Noise Voltage Distribution @ 10 kHz

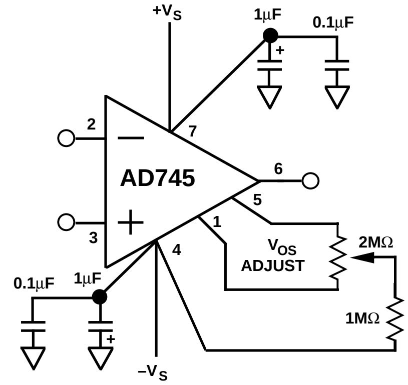


Figure 21. Offset Null Configuration, 8-Pin Package Pinout

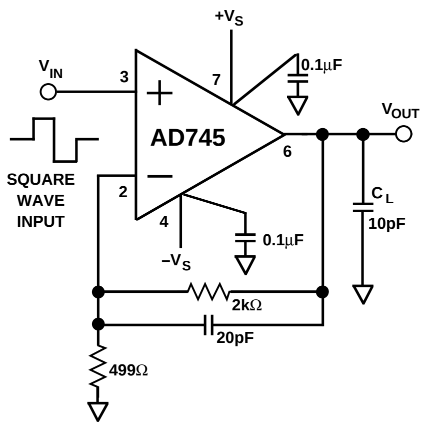


Figure 22a. Gain of 5 Follower, 8-Pin Package Pinout

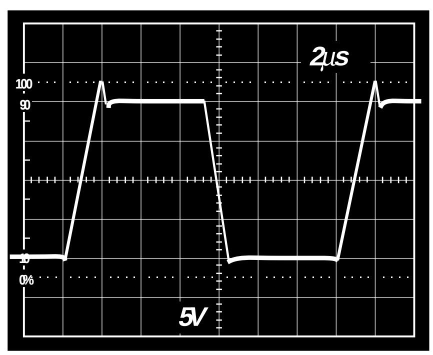


Figure 22b. Gain of 5 Follower Large Signal Pulse Response

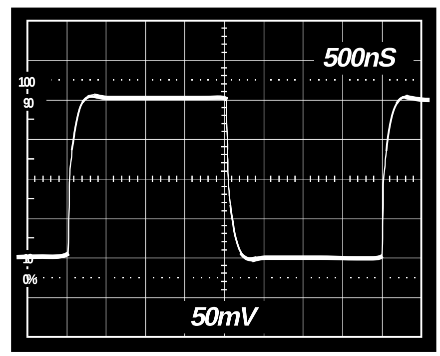


Figure 22c. Gain of 5 Follower Small Signal Pulse Response

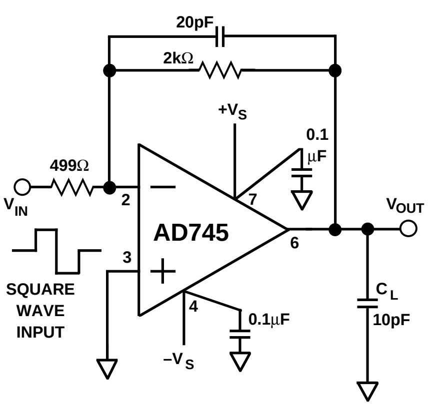


Figure 23a. Gain of 4 Inverter, 8-Pin Package Pinout

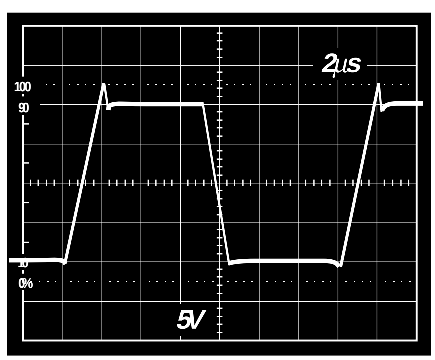


Figure 23b. Gain of 4 Inverter Large Signal Pulse Response

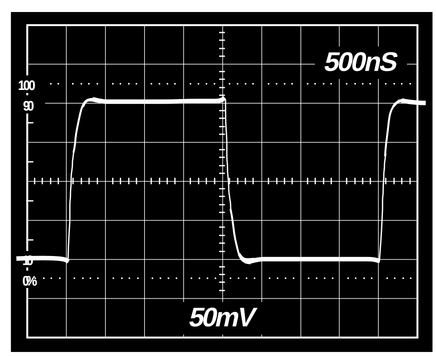


Figure 23c. Gain of 4 Inverter Small Signal Pulse Response

OP AMP PERFORMANCE JFET VS. BIPOLAR

The AD745 offers the low input voltage noise of an industry standard bipolar op amp without its inherent input current errors. This is demonstrated in Figure 24, which compares input voltage noise vs. input source resistance of the OP37 and the AD745 op amps. From this figure, it is clear that at high source impedance the low current noise of the AD745 also provides lower total noise. It is also important to note that with the AD745 this noise reduction extends all the way down to low source impedances. The lower dc current errors of the AD745 also reduce errors due to offset and drift at high source impedances (Figure 25).

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier, where low level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains.

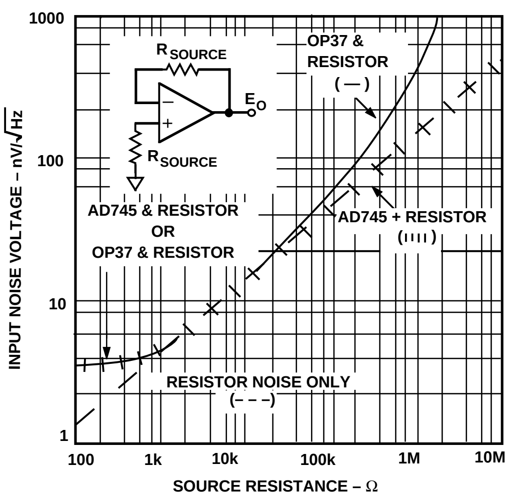


Figure 24. Total Input Noise Spectral Density @ 1 kHz vs. Source Resistance

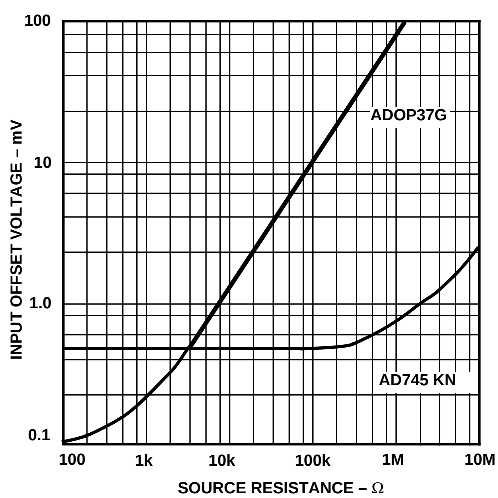


Figure 25. Input Offset Voltage vs. Source Resistance

DESIGNING CIRCUITS FOR LOW NOISE

An op amp's input voltage noise performance is typically divided into two regions: flatband and low frequency noise. The AD745 offers excellent performance with respect to both. The figure of 2.9 nV/√Hz @ 10 kHz is excellent for a JFET input amplifier. The 0.1 Hz to 10 Hz noise is typically 0.38 μV p-p. The user should pay careful attention to several design details in order to optimize low frequency noise performance. Random air currents can generate varying thermocouple voltages that appear as low frequency noise: therefore sensitive circuitry should be well shielded from air flow. Keeping absolute chip temperature low also reduces low frequency noise in two ways: first, the low frequency noise is strongly dependent on the ambient temperature and increases above +25°C. Secondly, since the gradient of temperature from the IC package to ambient is greater, the noise generated by random air currents, as previously mentioned, will be larger in magnitude. Chip temperature can be reduced both by operation at reduced supply voltages and by the use of a suitable clip-on heat sink, if possible.

Low frequency current noise can be computed from the magnitude of the dc bias current $\left(\tilde{I}_n = \sqrt{2qI_B\Delta f}\right)$ and increases below approximately 100 Hz with a 1/f power spectral density. For the AD745 the typical value of current noise is 6.9 fA/√Hz at 1 kHz. Using the formula, $\tilde{I}_n = \sqrt{4kT/R\Delta f}$, to compute the Johnson noise of a resistor, expressed as a current, one can see that the current noise of the AD745 is equivalent to that of a $3.45 \times 10^8\ \Omega$ source resistance.

At high frequencies, the current noise of a FET increases proportionately to frequency. This noise is due to the "real" part of the gate input impedance, which decreases with frequency. This noise component usually is not important, since the voltage noise of the amplifier impressed upon its input capacitance is an apparent current noise of approximately the same magnitude.

In any FET input amplifier, the current noise of the internal bias circuitry can be coupled externally via the gate-to-source capacitances and appears as input current noise. This noise is totally correlated at the inputs, so source impedance matching will tend to cancel out its effect. Both input resistance and input capacitance should be balanced whenever dealing with source capacitances of less than 300 pF in value.

LOW NOISE CHARGE AMPLIFIERS

As stated, the AD745 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones. When dealing with a high source capacitance, it is useful to consider the total input charge uncertainty as a measure of system noise.

Charge (Q) is related to voltage and current by the simply stated fundamental relationships:

$$Q = CV \text{ and } I = \frac{dQ}{dt}$$

As shown, voltage, current and charge noise can all be directly related. The change in open circuit voltage (ΔV) on a capacitor will equal the combination of the change in charge (ΔQ/C) and the change in capacitance with a built-in charge (Q/ΔC).

Figures 26 and 27 show two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier which has a very high input impedance, such as the AD745. Figure 26 shows a model of a charge amplifier circuit. Here, amplification depends on the principle of conservation of charge at the input of amplifier A1, which requires that the charge on capacitor C_S be transferred to capacitor C_F, thus yielding an output voltage of $\Delta Q/C_F$. The amplifiers input voltage noise will appear at the output amplified by the noise gain $(1 + (C_S/C_F))$ of the circuit.

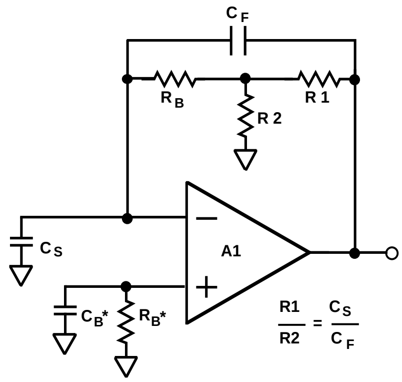


Figure 26. A Charge Amplifier Circuit

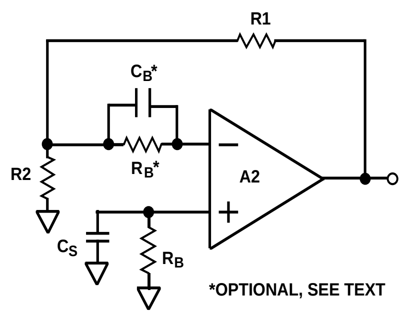


Figure 27. Model for A High Z Follower with Gain

The second circuit, Figure 27, is simply a high impedance follower with gain. Here the noise gain $(1 + (R1/R2))$ is the same as the gain from the transducer to the output. Resistor R_B, in both circuits, is required as a dc bias current return.

There are three important sources of noise in these circuits. Amplifiers A1 and A2 contribute both voltage and current noise, while resistor R_B contributes a current noise of:

$$\tilde{N} = \sqrt{4\,k\,\frac{T}{R_B}\,\Delta f}$$

where:

k = Boltzman's Constant = 1.381×10^{-23} Joules/Kelvin

T = Absolute Temperature, Kelvin (0°C = +273.2 Kelvin)

Δf = Bandwidth – in Hz (Assuming an Ideal "Brick Wall" Filter)

This must be root-sum-squared with the amplifier's own current noise.

Figure 28 shows that these two circuits have an identical frequency response and the same noise performance (provided that $C_S/C_F = R1/R2$). One feature of the first circuit is that a "T" network is used to increase the effective resistance of R_B and improve the low frequency cutoff point by the same factor.

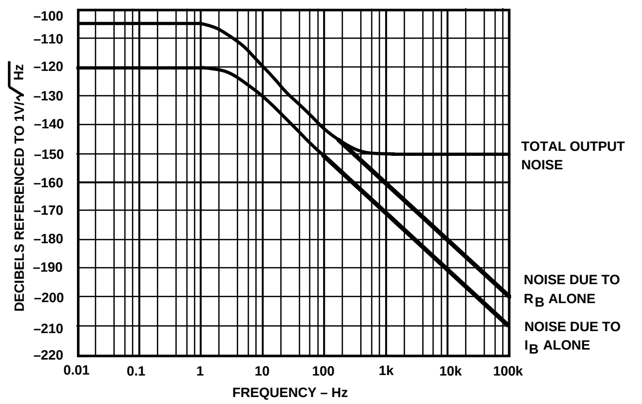


Figure 28. Noise at the Outputs of the Circuits of Figures 26 and 27. Gain = 10, C_S = 3000 pF, R_B = 22 MΩ

However, this does not change the noise contribution of R_B which, in this example, dominates at low frequencies. The graph of Figure 29 shows how to select an R_B large enough to minimize this resistor's contribution to overall circuit noise. When the equivalent current noise of R_B $((\sqrt{4\,kT})/R)$ equals the noise of $I_B\left(\sqrt{2qI_B}\right)$, there is diminishing return in making R_B larger.

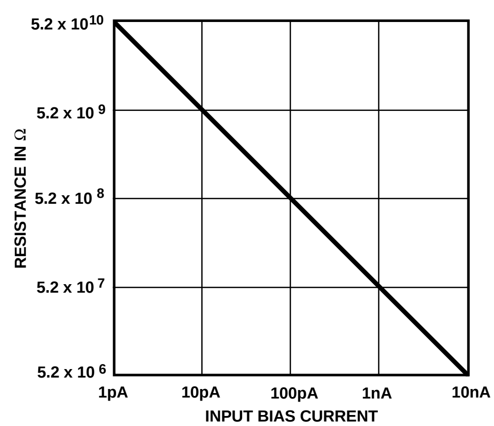


Figure 29. Graph of Resistance vs. Input Bias Current Where the Equivalent Noise $\sqrt{4\,kT/R}$, Equals the Noise of the Bias Current $I_B\left(\sqrt{2qI_B}\right)$

To maximize dc performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the optional resistor R_B in Figures 26 and 27. As previously mentioned, for best noise performance care should be taken to also balance the source capacitance designated by C_B The value for C_B in Figure 26 would be equal to C_S in Figure 27. At values of C_B over 300 pF, there is a diminishing impact on noise; capacitor C_B can then be simply a large mylar bypass capacitor of 0.01 µF or greater.

HOW CHIP PACKAGE TYPE AND POWER DISSIPATION AFFECT INPUT BIAS CURRENT

As with all JFET input amplifiers, the input bias current of the AD745 is a direct function of device junction temperature, I_B approximately doubling every 10°C. Figure 30 shows the relationship between bias current and junction temperature for the AD745. This graph shows that lowering the junction temperature will dramatically improve I_B.

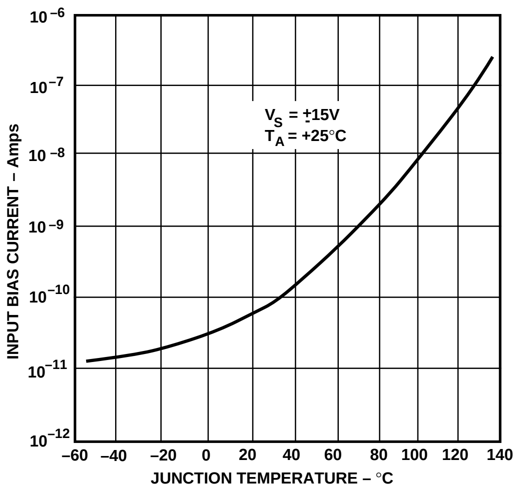


Figure 30. Input Bias Current vs. Junction Temperature

The dc thermal properties of an IC can be closely approximated by using the simple model of Figure 31 where current represents power dissipation, voltage represents temperature, and resistors represent thermal resistance (θ in °C/watt).

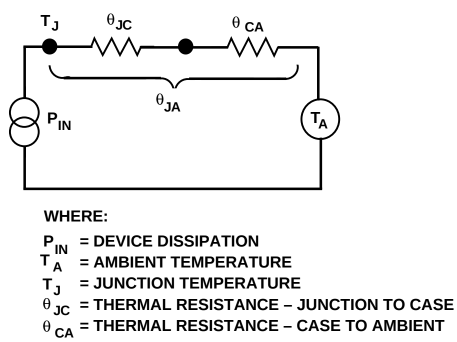


Figure 31. Device Thermal Model

From this model $T_J = T_A + \theta_{JA} P_{IN}$. Therefore, I_B can be determined in a particular application by using Figure 30 together with the published data for θ_{JA} and power dissipation. The user can modify θ_{JA} by use of an appropriate clip-on heat sink such as the Aavid #5801. θ_{JA} is also a variable when using the AD745 in chip form. Figure 32 shows bias current vs. supply voltage with θ_{JA} as the third variable. This graph can be used to predict bias current after θ_{JA} has been computed. Again bias current will double for every 10°C. The designer using the AD745 in chip form (Figure 33) must also be concerned with both θ_{JC} and θ_{CA}, since θ_{JC} can be affected by the type of die mount technology used.

Typically, θ_{JC}'s will be in the 3°C to 5°C/watt range; therefore, for normal packages, this small power dissipation level may be ignored. But, with a large hybrid substrate, θ_{JC} will dominate proportionately more of the total θ_{JA}.

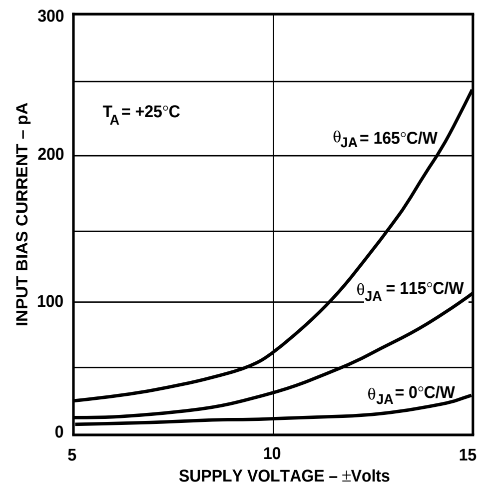


Figure 32. Input Bias Current vs. Supply Voltage for Various Values of θ_{JA}

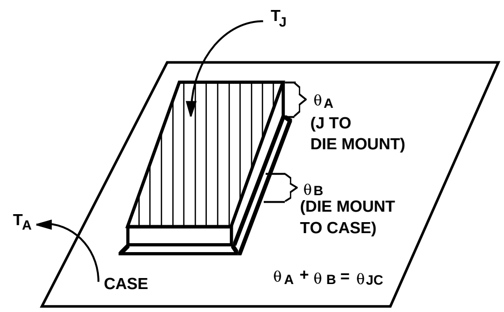


Figure 33. Breakdown of Various Package Thermal Resistance

REDUCED POWER SUPPLY OPERATION FOR LOWER I_B

Reduced power supply operation lowers I_B in two ways: first, by lowering both the total power dissipation and, second, by reducing the basic gate-to-junction leakage (Figure 32). Figure 34 shows a 40 dB gain piezoelectric transducer amplifier, which operates without an ac coupling capacitor, over the –40°C to +85°C temperature range. If the optional coupling capacitor, C1, is used, this circuit will operate over the entire –55°C to +125°C temperature range.

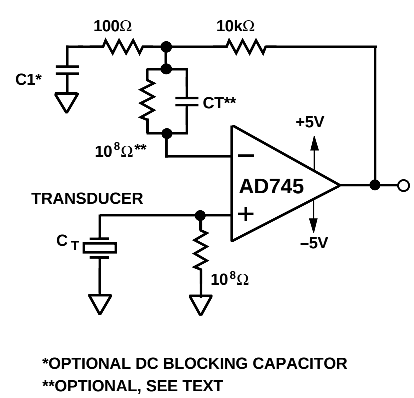


Figure 34. A Piezoelectric Transducer

TWO HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

Two of the most popular charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output (pC/g).* Figures 35a and 35b show two ways in which to configure the AD745 as a low noise charge amplifier for use with a wide variety of piezoelectric accelerometers. The input sensitivity of these circuits will be determined by the value of capacitor C1 and is equal to:

$$\Delta V_{OUT} = \frac{\Delta Q_{OUT}}{C1}$$

The ratio of capacitor C1 to the internal capacitance (C_T) of the transducer determines the noise gain of this circuit ($1 + C_T/C1$). The amplifiers voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor R1. If a "T" network is used, the effective value is: R1 (1 + R2/R3).

*pC = Picocoulombs
g = Earth's Gravitational Constant

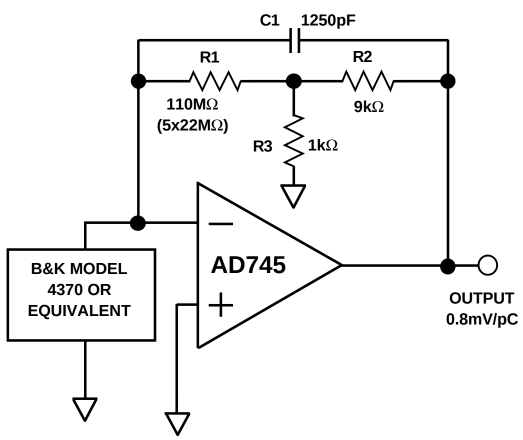


Figure 35a. A Basic Accelerometer Circuit

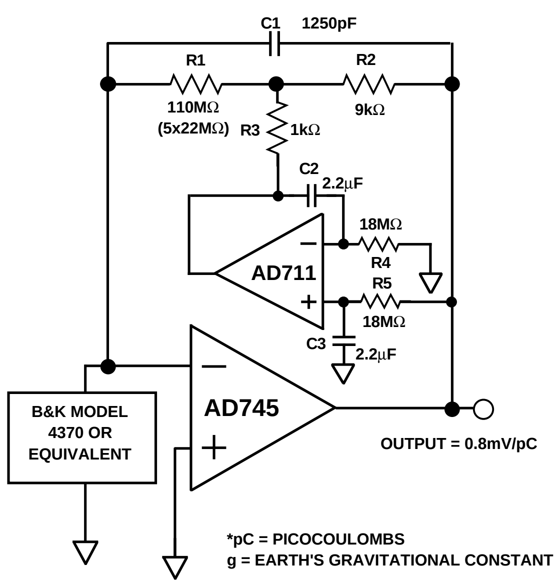


Figure 35b. An Accelerometer Circuit Employing a DC Servo Amplifier

A dc servo loop (Figure 35b) can be used to assure a dc output <10 mV, without the need for a large compensating resistor when dealing with bias currents as large as 100 nA. For optimal low frequency performance, the time constant of the servo loop (R4C2 = R5C3) should be:

$$\text{Time Constant} \geq 10\ R1\left(1+\frac{R2}{R3}\right)C1$$

A LOW NOISE HYDROPHONE AMPLIFIER

Hydrophones are usually calibrated in the voltage-out mode. The circuit of Figures 36a can be used to amplify the output of a typical hydrophone. If the optional ac coupling capacitor C_C is used, the circuit will have a low frequency cutoff determined by an RC time constant equal to:

$$\text{Time Constant} = \frac{1}{2\pi \times C_C \times 100\ \Omega}$$

where the dc gain is 1 and the gain above the low frequency cutoff ($1/(2\pi\ C_C(100\ \Omega))$) is equal to (1 + R2/R3). The circuit of Figure 36b uses a dc servo loop to keep the dc output at 0 V and to maintain full dynamic range for I_B's up to 100 nA. The time constant of R7 and C1 should be larger than that of R1 and C_T for a smooth low frequency response.

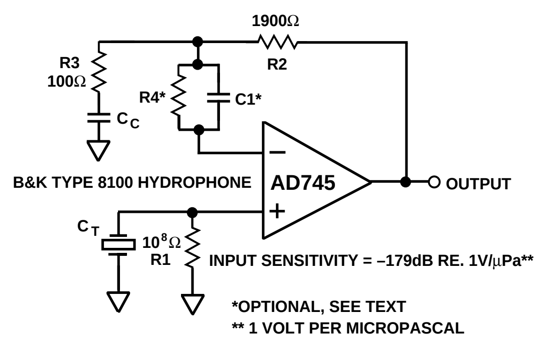


Figure 36a. A Low Noise Hydrophone Amplifier

The transducer shown has a source capacitance of 7500 pF. For smaller transducer capacitances (≤300 pF), lowest noise can be achieved by adding a parallel RC network (R4 = R1, C1 = C_T) in series with the inverting input of the AD745.

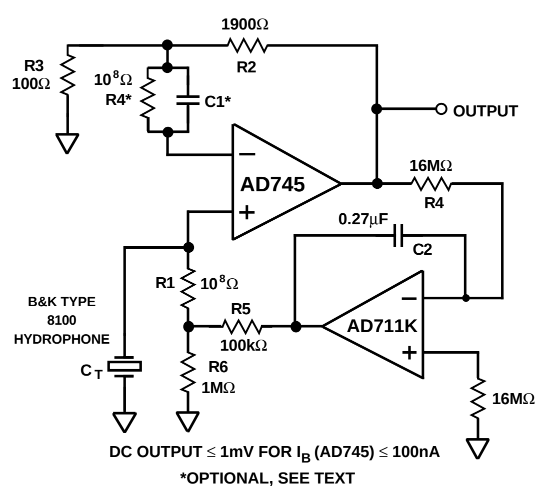


Figure 36b. A Hydrophone Amplifier Incorporating a DC Servo Loop

Design Considerations for I-to-V Converters

There are some simple rules of thumb when designing an I-V converter where there is significant source capacitance (as with a photodiode) and bandwidth needs to be optimized. Consider the circuit of Figure 37. The high frequency noise gain ($1 + C_S/C_L$) is usually greater than five, so the AD745, with its higher slew rate and bandwidth is ideally suited to this application.

Here both the low current and low voltage noise of the AD745 can be taken advantage of, since it is desirable in some instances to have a large R_F (which increases sensitivity to input current noise) and, at the same time, operate the amplifier at high noise gain.

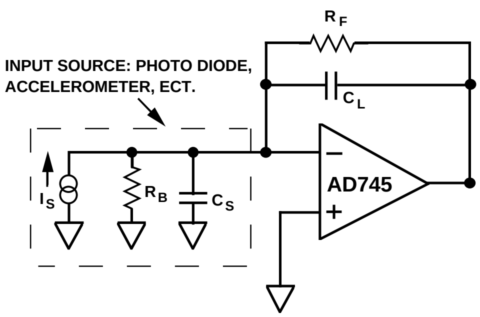


Figure 37. A Model for an I-to-V Converter

In this circuit, the R_F C_S time constant limits the practical bandwidth over which flat response can be obtained, in fact:

$$f_B \approx \sqrt{\frac{f_C}{2\pi R_F C_S}}$$

where:

f_B = signal bandwidth

f_C = gain bandwidth product of the amplifier

With $C_L \approx 1/(2\ \pi\ R_F\ C_S)$ the net response can be adjusted to a provide a two pole system with optimal flatness that has a corner frequency of f_B. Capacitor C_L adjusts the damping of the circuit's response. Note that bandwidth and sensitivity are directly traded off against each other via the selection of R_F. For example, a photodiode with C_S = 300 pF and R_F = 100 kΩ will have a maximum bandwidth of 360 kHz when capacitor $C_L \approx 4.5$ pF. Conversely, if only a 100 kHz bandwidth were required, then the maximum value of R_F would be 360 kΩ and that of capacitor C_L still ≈ 4.5 pF.

In either case, the AD745 provides impedance transformation, the effective transresistance, i.e., the I/V conversion gain, may be augmented with further gain. A wideband low noise amplifier such as the AD829 is recommended in this application.

This principle can also be used to apply the AD745 in a high performance audio application. Figure 38 shows that an I-V converter of a high performance DAC, here the AD1862, can be designed to take advantage of the low voltage noise of the AD745 (2.9 nV/$\sqrt{Hz}$) as well as the high slew rate and bandwidth provided by decompensation. This circuit, with component values shown, has a 12 dB/octave rolloff at 728 kHz, with a passband ripple of less than 0.001 dB and a phase deviation of less than 2 degrees @ 20 kHz.

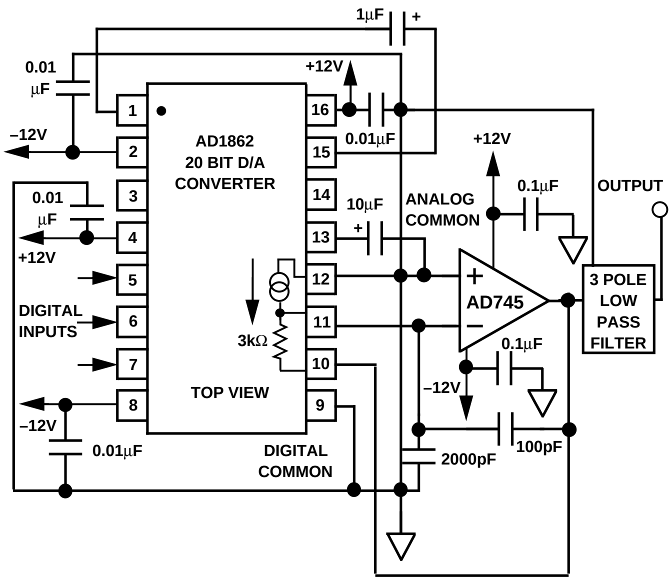


Figure 38. A High Performance Audio DAC Circuit

An important feature of this circuit is that high frequency energy, such as clock feedthrough, is shunted to common via a high quality capacitor and not the output stage of the amplifier, greatly reducing the error signal at the input of the amplifier and subsequent opportunities for intermodulation distortions.

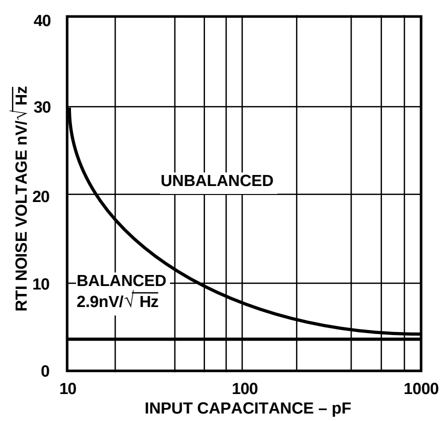


Figure 39. RTI Noise Voltage vs. Input Capacitance

BALANCING SOURCE IMPEDANCES

As mentioned previously, it is good practice to balance the source impedances (both resistive and reactive) as seen by the inputs of the AD745. Balancing the resistive components will optimize dc performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing input capacitance will minimize ac response errors due to the amplifier's input capacitance and, as shown in Figure 39, noise performance will be optimized. Figure 40 shows the required external components for noninverting (A) and inverting (B) configurations.

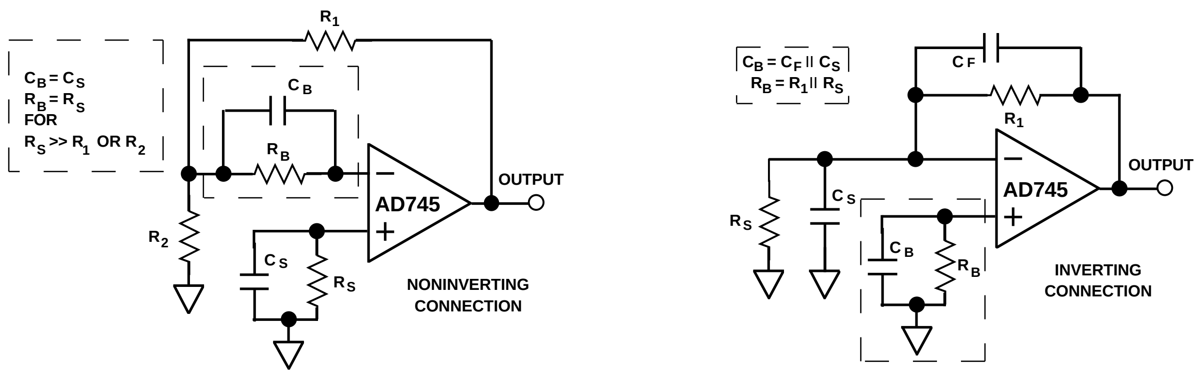


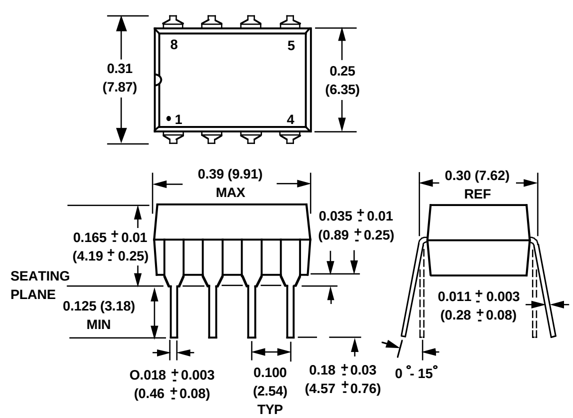
Figure 40. Optional External Components for Balancing Source Impedances

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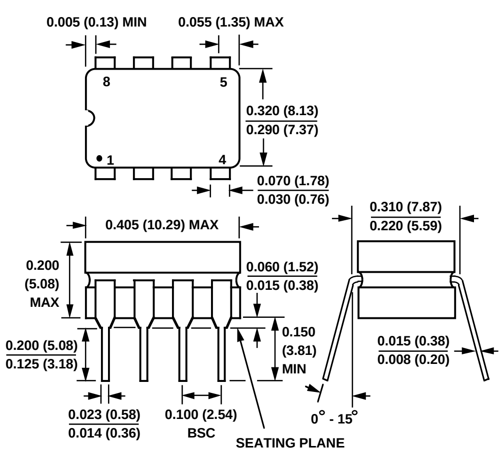
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

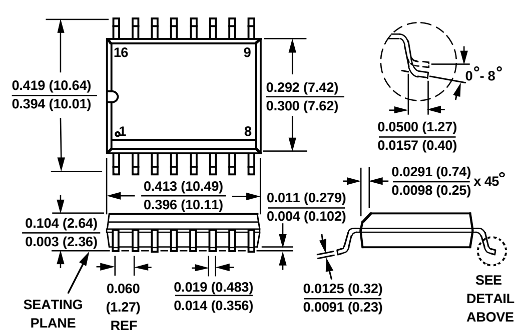
8-Pin Plastic Mini-DIP (N) Package



8-Pin Cerdip (Q) Package



16-Pin SOIC (R) Package



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